IN THE CLAIMS:

Claims 1, 6 and 25 have been amended herein. All of the pending claims 1 through 25 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

1. (Currently amended) A method of assembling a ~~flip-chip~~ flip chip-type semiconductor device assembly, the method comprising:

providing a wafer having an active surface and a back surface and including a plurality of unsingulated semiconductor dice, at least some semiconductor dice of the plurality having conductive bumps protruding transversely from the active surface;

providing a wafer scale interposer substrate having a first surface and a second surface, the wafer scale interposer substrate including a plurality of unsingulated interposer substrates, each having a plurality of conductive elements thereon adjacent the second surface, each unsingulated interposer substrate dimensioned and located to correspond with one of the plurality of semiconductor dice of the wafer, each of the plurality of interposer substrates having a plurality of recesses extending thereinto from the first surface to expose at least a portion of one of the plurality of conductive elements; and

placing the wafer with the active surface thereof facing the first surface of the wafer scale interposer substrate and the plurality of unsingulated semiconductor dice in alignment with the plurality of unsingulated interposer substrates and disposing each of the conductive bumps protruding transversely from the active surface into a recess of the plurality of recesses of the plurality of interposer substrates so that the conductive bumps are substantially received within the plurality of recesses in the plurality of interposer substrates.

2. (Previously presented) The method of claim 1, further comprising attaching the active surface of the wafer directly to the first surface of the wafer scale interposer substrate by at least one adhesive element disposed on the first surface at a location of each of the plurality of interposer substrates.

3. (Previously presented) The method of claim 1, wherein disposing comprises abutting the active surface of the wafer with the first surface of the wafer scale interposer substrate.

4. (Previously presented) The method of claim 1, further comprising aligning each of the conductive bumps on the at least some semiconductor dice with the plurality of recesses so that each of the conductive bumps is positioned directly over one of the plurality of recesses.

5. (Previously presented) The method of claim 1, wherein providing the wafer scale interposer substrate comprises forming the plurality of recesses to be sized and configured to substantially receive the conductive bumps therein.

6. (Currently amended) The method of claim 1, wherein providing the wafer scale interposer substrate comprises forming the plurality of recesses collectively in each of the semiconductor dice in at least one of a centrally aligned row configuration, a peripheral ~~configuration~~ configuration, and an I-shaped configuration.

7. (Previously presented) The method of claim 1, wherein disposing comprises positioning the conductive bumps of the plurality of semiconductor dice in the recesses of the plurality of an interposer substrate so that a surface of each of the conductive bumps directly contacts a respective conductive element of the plurality of conductive elements.

8. (Previously presented) The method of claim 1, further comprising bonding the conductive bumps to the plurality of conductive elements, respectively.

9. (Previously presented) The method of claim 8, wherein bonding comprises bonding by at least one of reflowing, curing, ultrasonic bonding and thermal compression bonding.

10. (Previously presented) The method of claim 1, further comprising disposing a nonsolid conductive material on the conductive bumps prior to disposing the conductive bumps in the plurality of recesses.

11. (Previously presented) The method of claim 10, further comprising bonding each of the conductive bumps having the nonsolid conductive material thereon to each of the plurality of conductive elements using the nonsolid material.

12. (Previously presented) The method of claim 1, further comprising disposing a nonsolid conductive material in each of the plurality of recesses.

13. (Previously presented) The method of claim 12, wherein disposing the nonsolid conductive material comprises:

providing a stencil having a pattern of apertures therethrough corresponding to a pattern of the plurality of recesses of the plurality of unsingulated interposer substrates of the wafer scale interposer substrate;

positioning the stencil over the wafer scale interposer substrate so that the pattern of apertures corresponds with the pattern of the plurality of recesses; and

spreading the nonsolid conductive material over the stencil and into the plurality of recesses with a spreading member.

14. (Previously presented) The method of claim 12, further comprising inserting each of the conductive bumps in a recess of the plurality of recesses in contact with the nonsolid conductive material therein.

15. (Previously presented) The method of claim 14, further comprising bonding each of the conductive bumps inserted in the plurality of recesses to the plurality of conductive elements using the nonsolid conductive material.

16. (Previously presented) The method of claim 1, wherein providing the wafer scale interposer substrate comprises providing the wafer scale interposer substrate with at least one opening in the first surface thereof at a location of each interposer substrate and placing and configuring the at least one opening to communicate with at least one recess of the plurality of recesses.

17. (Previously presented) The method of claim 16, further comprising introducing dielectric filler material through the at least one opening into a space adjacent the conductive bumps in the at least one recess.

18. (Previously presented) The method of claim 1, further comprising introducing dielectric filler material into a space adjacent at least some of the conductive bumps disposed in the plurality of recesses.

19. (Previously presented) The method of claim 1, wherein providing the wafer comprises providing a layer of encapsulation material on the back surface thereof.

20. (Previously presented) The method of claim 19, wherein providing the layer of the encapsulation material is effected by at least one of spin-coating and glob-top covering.

21. (Previously presented) The method of claim 18, further comprising dicing the wafer and the wafer scale interposer substrate into singulated semiconductor device assemblies, each of the singulated semiconductor device assemblies comprising at least one semiconductor die of the plurality of semiconductor dice secured to at least one interposer substrate of the plurality of interposer substrates.

22. (Previously presented) The method of claim 21, further comprising at least partially encapsulating the singulated semiconductor device assemblies by dispensing encapsulation material about a periphery of the at least one semiconductor die of each of the singulated semiconductor device assemblies.

23. (Previously presented) The method of claim 1, further comprising dicing the wafer disposed to the wafer scale interposer substrate into singulated semiconductor device assemblies, each of the singulated semiconductor assemblies comprising at least one semiconductor die of the plurality of semiconductor dice secured to at least one interposer substrate of the plurality of interposer substrates.

24. (Previously presented) The method of claim 23, further comprising at least partially encapsulating the singulated semiconductor assemblies by dispensing encapsulation material about a periphery of the at least one semiconductor die of each of the singulated semiconductor device assemblies.

25. (Currently amended) The method of claim 24, wherein the at least partially encapsulating the singulated semiconductor device ~~assembles~~ assemblies comprises leaving the back surface of the at least one semiconductor die exposed.